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INFORMATION DISCLOSURE CITATION (Use Several Sheets if Necessary)				APPLICANTS Lester J. Kozlowski et al.		RECEIVED	
				FILING DATE April 24, 2000		GROUP ART UNIT JUL 26 2000	
U. S. PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
							
FOREIGN PATENT DOCUMENTS							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
YES	NO						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
KJ	AA	CMOS: Circuit Design, Layout, and Simulation; R. Jacob Baker, Harry W. Li and David E. Boyce, 1998, Chpt. 2-4.					
KJ	BB	Integrated Circuit Manufacturability, The Art of Process and Design Integration, Dhiraj K. Pradhan, 1999, Chpt. 4-5.					
EXAMINER		<i>Kelly J. Q.</i>		DATE CONSIDERED		9/9/05	
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.							